Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) A method for processing data using a plurality of processing engines, the method comprising:

processing first data associated with a younger control record in a first processing engine;

processing second data associated with an older control record in a second processing engine;

enabling a first interrupt indicator in [[a]] the younger control record;

if processing of the first data completes before processing of the second data completes, moving the first interrupt indicator associated with the younger control record onto a second interrupt indicator associated with the older control record, wherein moving the first interrupt indicator comprises setting the first interrupt indicator associated with the younger control record to disabled and setting the second interrupt indicator associated with the older control record to enabled; and

if processing of the first data completes after processing of the second data completes, generating an interrupt when processing of the first data completes.

2. (Original) The method of claim 1, wherein the first processing engine is a public key engine.

3. (Previously Presented) The method of claim 1, wherein moving the first interrupt indicator comprises determining that the first interrupt indicator is enabled.

4. (Previously Presented) The method of claim 1, wherein moving the first interrupt indicator comprises delaying the generation of an interrupt associated with the younger control record.

5-7. (Cancelled)

8. (Original) The method of claim 1, wherein the older control record comprises a reference to data.

9. (Original) The method of claim 8, wherein the older control record comprises a reference to an operation to be performed on data.

10. (Original) The method of claim 1, further comprising writing processed data to memory associated with a host.

11. (Previously Presented) The method of claim 10, wherein the host is an external processor coupled to the processing engines.

12. (Previously Presented) The method of claim 11, wherein the external processor is coupled to the processing engines through a scheduler.

13. (Canceled)

14. (Previously Presented) The method of claim 12, wherein the external processor reads the processed data when the interrupt is generated.

15. (Currently Amended) A cryptography accelerator, comprising:

an interface coupled to an external processor and memory associated with the external processor;

a first processing engine coupled to the interface, the first processing engine configured to receive a first control record from the external processor;

a second processing engine coupled to the interface, the second processing engine configured to receive a second control record from the external processor;

a history buffer containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record;

wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record completes;

wherein an interrupt is generated when processing of the first control record completes if processing of the first control record completes after processing of the second control record completes; and

wherein moving the first interrupt indicator comprises setting the first interrupt indicator associated with the ~~younger~~ first control record to disabled and setting the second interrupt indicator associated with the [[older]] second control record to enabled.

16. (Original) The cryptography accelerator of claim 15, wherein the first processing engine is a public key engine.

17. (Cancelled)

18. (Currently Amended) The cryptography accelerator of claim [[17]] 15, wherein ~~collapsing~~ moving the first interrupt indicator associated with the first control record onto the second control record further comprises delaying the generation of an interrupt associated with the first control record.

19-21. (Cancelled)

22. (Original) The cryptography accelerator of claim 15, wherein the second control record comprises a reference to data.

23. (Original) The cryptography accelerator of claim 22, wherein the second control record comprises a reference to an operation to be performed on data.

24. (Previously Presented) The cryptography accelerator of claim 23, wherein the external processor is coupled to the processing engines through a scheduler.

25. (Canceled)

26. (Previously Presented) The cryptography accelerator of claim 24, wherein the external processor reads the processed data when the interrupt is generated.

27-42. (Cancelled)